IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Douglas D. Coolbaugh, et al.	**Examiner**:	Samuel A. Gebremariam
Serial No:	10/707,065	**Art Unit**:	2811
Filed:	November 19, 2003	**Docket**:	BUR920020116US1 (16512)
For:	TRI-METAL AND DUAL-METAL STACKED INDUCTORS	**Dated**:	June 20, 2006

Confirmation No.: 1064

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
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RESPONSE UNDER 37 C.F.R. § 1.111

Dear Sir:

In response to the Advisory Action dated June 8, 2006 and the Office Action dated March 20, 2006, applicants submit the following amendments and remarks for entry of record in the above-identified patent application. This Response is filed in conjunction with a Request for Continued Examination (RCE).

CERTIFICATE OF ELECTRONIC TRANSMISSION

I hereby certify that this correspondence is being filed electronically to the U.S. Patent and Trademark Office.

Dated: June 20, 2006

Leslie S. Szivos, Ph.D.

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) A semiconductor structure comprising a high performance metal stacked inductor having a relatively low sheet resistance, said metal stacked inductor comprising at least one first layer of metal embedded within a dielectric material, said first layer of metal serving ~~which serves~~ as an upper metal wire in the semiconductor structure and a second layer of metal located directly on top of the first layer of metal and above said dielectric material, wherein said first layer of metal is in electrical contact with a lower metal wire by a via, and said first layer of metal and said second layer of metal are not interconnected by a via.

2. (Previously Presented) The semiconductor structure of Claim 1 further comprising a third metal layer located directly on top of the second layer of metal, wherein said second layer of metal and said third layer of metal are not interconnected by a via.

3. (Original) The semiconductor structure of Claim 1 wherein the metal stacked inductor is spiral shaped.

4. (Original) The semiconductor structure of Claim 2 wherein the metal stacked inductor is spiral shaped.

5. (Cancelled)

6. (Currently Amended) The semiconductor structure of Claim [[5]] 1 wherein said lower metal ~~wiring level~~ wire is ~~comprises a wiring region~~ embedded within an interconnect dielectric.

7. (Previously Presented) The semiconductor structure of Claim 2 further comprising at least one wiring region that lies to the periphery of the metal stacked inductor, wherein in the at least one wiring region the second layer of metal serves as a via interconnecting two metal wires.

8. (Original) The semiconductor structure of Claim 1 wherein the first layer of metal is comprised of a low resistivity conductive material having a resistivity of about 3.0 micro-ohm*cm or less.

9. (Original) The semiconductor structure of Claim 8 wherein the low resistivity conductive material is selected from the group consisting of Cu, Al, Pt, Ag, Au, and alloys thereof.

10. (Original) The semiconductor structure of Claim 8 wherein the low resistivity conductive material is Cu.

11. (Original) The semiconductor structure of Claim 1 wherein the second layer of metal is comprised of a low resistivity conductive material having a resistivity of about 3 micro-ohm*cm or less, said second layer of metal comprising the same or different conductive material as the first layer of metal.

12. (Original) The semiconductor structure of Claim 11 wherein the low resistivity conductive material is selected from the group consisting of Cu, Al, Pt, Ag, Au, and alloys thereof.

13. (Original) The semiconductor structure of Claim 11 wherein the low resistivity conductive material is Al or Cu.

14. (Original) The semiconductor structure of Claim 2 wherein the third layer of metal is comprised of a low resistivity conductive material having a resistivity of about 3 micro- ohm*cm or less, said third layer of metal comprising the same or different conductive material as the first or second layers of metal.

15. (Original) The semiconductor structure of Claim 14 wherein the low resistivity conductive material is selected from the group consisting of Cu, Al, Pt, Ag, Au, and alloys thereof.

16. (Original) The semiconductor structure of Claim 14 wherein the low resistivity conductive material is Al.

17. (Original) The semiconductor structure of Claim 1 wherein the first layer of metal is comprised of Cu and the second layer of metal is comprised of Al.

18. (Original) The semiconductor structure of Claim 2 wherein the first layer of metal is comprised of Cu, the second layer of metal is comprised of Cu and the third layer of metal is comprised of Al.

19. (Currently Amended) A method of forming a semiconductor structure comprising:

providing a partial interconnect structure comprising a lower metal wiring level located on a substrate;

forming a ~~first~~ dielectric material on the partial interconnect structure;

forming a first layer of metal in said ~~first~~ dielectric material, said first layer of metal serves as an upper metal wire of the interconnect structure and as the bottom layer of a metal stacked inductor, wherein said first layer of metal is in electrical contact with a lower metal wire by a via; and

forming a second layer of metal on said first metal layer and above said dielectric material, wherein said first layer of metal and said second layer of metal are not interconnected by a via.

20. (Previously Presented) The method of Claim 19 further comprising forming a third layer of metal directly on top of the second layer of metal, wherein said second layer of metal and said third layer of metal are not interconnected by a via.

REMARKS

Favorable reconsideration of this application in view of the amendments and the remarks to follow and allowance of the claims of the present application are respectfully requested.

Applicants have amended Claim 1 to positively recite that the claimed metal stacked inductor comprises at least one first layer of metal *embedded within a dielectric material*, said first layer of metal serving as an upper metal wire in the semiconductor structure and a second layer of metal located directly on top of the first layer of metal *and above said dielectric material*. Support for these amendments to Claim 1 can be found in FIG. 4E and related processing details. In FIG. 4E, reference numeral 52 is the first layer of metal embedded within dielectric material 58. The second layer of metal 54 is located directly atop the first layer of metal 52 and above the dielectric material 58.

In a similar manner, applicants have amended Claim 19 to positively recite a step of "forming a second layer of metal on said first metal layer *and above said dielectric material*, wherein said first layer of metal and said second layer of metal are not interconnected by a via." Support for this amendment to Claim 19 is also found in the processing details of the present application as well as in FIG. 4E.

Applicants have also cancelled Claim 5 and made minor amendments to Claim 6.

Since the amendments to the claims do not introduce any new matter into the present application, entry thereof is respectfully requested.

In the Final Rejection dated March 20, 2006, Claims 1-9 and 19-20 were rejected under 35 U.S.C. § 102(b) as allegedly anticipated by U.S. Patent No. 6,287,931 to Chen ("Chen").

It is axiomatic that anticipation under §102 requires that the prior art reference disclose each and every element of the claim to which it is applied. *In re King*, 801 F.2d, 1324, 1326, 231

USPQ 136, 138 (Fed. Cir. 1996). Thus, there must be no differences between the subject matter of the claim and the disclosure of the prior art reference.

Applicants respectfully submit that Claims 1-9 are not anticipated by the disclosure of Chen since the applied reference does not disclose the claimed structure, as recited in amended Claim 1. Specifically, Chen does not disclose a semiconductor structure comprising a high performance metal stacked inductor having a relatively low sheet resistance, said metal stacked inductor comprising at least one first layer of metal *embedded within a dielectric material, said first layer of metal serving as an upper metal wire in the semiconductor structure and a second layer of metal located directly on top of the first layer of metal and above said dielectric material*, wherein said first layer of metal is in electrical contact with a lower metal wire by a via, and said first layer of metal and said second layer of metal are not interconnected by a via.

In contrast to the claimed structure, Chen discloses a structure in which the upper metal wire 32 is in contact with the spiral conductive coil 28 by via 30, and the spiral conductive coil 28 is in contact with the lower metal wire by via 26. Hence, each of the various metal levels are in contact with each by means of a via. Applicants observe that at Col, 4, lines 40-44, it is stated that "[F]or example, two or more metal layers can be stacked to implement the spiral conductive layer 28 to ...". This implies that within dielectric layer 33 or 29 the spiral inductor may comprise a stack of various metal layers. This section of Chen however does not disclose the claimed structure, as recited in amended Claim 1. In the claimed structure as amended above, the metal stacked inductor comprises at least one first layer of metal *embedded within a dielectric material*, said first layer of metal serving as an upper metal wire in the semiconductor structure and a second layer of metal located directly on top of the first layer of metal *and above said dielectric material*. As such, structure Claims 1-9 are not anticipated by Chen.

Applicants submit that method Claims19-20 are not anticipated by Chen as well since the applied reference does not teach or suggest the claimed method, as recited in Claim 19. Specifically, Chen does not teach or suggest a method including providing a partial interconnect structure comprising a lower metal wiring level located on a substrate; forming a dielectric material on the partial interconnect structure; forming a first layer of metal in said dielectric material, said first layer of metal serves as an upper metal wire of the interconnect structure and as the bottom layer of a metal stacked inductor, wherein said first layer of metal is in electrical contact with a lower metal wire by a via; and *forming a second layer of metal on said first metal layer and above said dielectric material, wherein said first layer of metal and said second layer of metal are not interconnected by a via*.

In contrast to the claimed method, Chen discloses a method in which a via 30 is formed in a dielectric material 29 to connect metal wire 32 to spiral coil 28. Via 26 is formed into dielectric 25 to connect the spiral coil 28 to metal wire 24. Applicants note that when the spiral inductor is formed of multiple metal layers, the multiple metal layers of the inductor are embedded within the same dielectric material. This is different from the claimed invention in which the first metal layer is embedded in a dielectric material and the second metal layer is formed directly on the first metal layer and above the dielectric material. As such, method Claims 19-20 are not anticipated by the disclosure of Chen.

The foregoing remarks clearly demonstrate that the applied reference does not teach each and every aspect of the claimed invention, as required by King and Kloster Speedsteel; therefore the claims of the present application are not anticipated by the disclosure of Chen. Applicants respectfully submit that the instant § 102 rejection has been obviated and withdrawal thereof is respectfully requested.

In the Final Rejection dated March 20, 2006, the following rejections were made: Claims 10 and 13 were rejected under 35 U.S.C. § 103 as allegedly unpatentable over the combined disclosures of Chen and U.S. Patent No. 6,639,298 to Chaudhry et al. ("Chaudhry et al."). Claims 11-12 and 14-15 were rejected as allegedly unpatentable over the combined disclosures of Chen and U.S. Patent Application Publication No. 2002/0125575 to Chaen ("Chaen"). Claim 16 was rejected under 35 U.S.C. § 103 as allegedly unpatentable over the combined disclosures of Chen, Chaen and U.S. Patent No. 6,395,637 to Park et al. ("Park et al."). Claim 17 was rejected under § 103 as allegedly unpatentable over the combined disclosures of Chen, and Park et al.

Applicants respectfully submit that the claimed structure as recited in Claim 1 of the present application is not rendered obvious by the combination of Chen and Chaudhry et al., Chen and Chaen, Chan, Chaen and Park et al. or Chan and Park et al. Specifically, none of the applied combination of references teaches or suggests a semiconductor structure comprising a high performance metal stacked inductor having a relatively low sheet resistance, said metal stacked inductor comprising at least one first layer of metal *embedded within a dielectric material, said first layer of metal serving as an upper metal wire in the semiconductor structure and a second layer of metal located directly on top of the first layer of metal and above said dielectric material*, wherein said first layer of metal is in electrical contact with a lower metal wire by a via, and said first layer of metal and said second layer of metal are not interconnected by a via.

The principal reference, i.e., Chan, spurring each of the obviousness rejections is defective since the applied reference discloses a stack inductor in which the multilayers of the stack inductor are embedded within the same dielectric material. In the claimed structure, the

metal stacked inductor comprises at least one first layer of metal *embedded within a dielectric material, said first layer of metal serving as an upper metal wire in the semiconductor structure and a second layer of metal located directly on top of the first layer of metal and above said dielectric material.* Such a metal stack inductor is not taught or suggest by Chan.

The applied secondary references of Chaudhry et al., Chaen and Park et al do not alleviate the above defect in Chan since those references also do not teach or suggest a metal stacked inductor that comprises at least one first layer of metal *embedded within a dielectric material, said first layer of metal serving as an upper metal wire in the semiconductor structure and a second layer of metal located directly on top of the first layer of metal and above said dielectric material.*

The various §103 rejections also fail because there is no motivation in the applied references which suggest modifying the disclosed structures include the various elements recited in the claims of the present invention. Thus, there is no motivation provided in the applied references, or otherwise of record, to make the modification mentioned above. "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." In re Vaeck, 947 F.2d, 488, 493, 20 USPQ 2d. 1438, 1442 (Fed.Cir. 1991).

The rejections under 35 U.S.C. §103 have been obviated; therefore reconsideration and withdrawal thereof is respectfully requested.

Thus, in view of the foregoing remarks, it is firmly believed that the present case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,

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